WHAT IS CLAIMED IS:

1. A demodulator for demodulating a set of S possible orthogonal modulation codes received serially as binary data, wherein each of said S possible orthogonal modulation codes comprises M binary bits representing an N-bit data symbol and wherein $M = 2^N$, said demodulator comprising:

a Logic 00 input detector, a Logic 01 input detector, a Logic 10 input detector and a Logic 11 input detector, wherein each of said Logic 00 input detector, said Logic 01 input detector, said Logic 10 input detector, and said Logic 11 input detector compares sequential pairs of said M binary bits of said serially received orthogonal modulation codes to a respective one of a Logic 00 value, a Logic 01 value, a Logic 10 value, and a Logic 11 value and outputs a [+1,+1] signal if a match occurs and outputs a [-1,-1] signal if a match does not occur;

a summation circuit comprising S accumulators;

a storage array capable of storing S Logic 00 code masks, each of said S Logic 00 code masks associated with one of said S possible orthogonal modulation codes, wherein a kth Logic 00 code mask comprises M/2 Logic 00 code mask bits, each of said M/2 Logic 00 code mask bits associated with a corresponding one of M/2 sequential pairs of M binary bits in a kth orthogonal modulation code, wherein said each M/2 Logic 00 code mask bit is a Logic 1 if

said corresponding sequential pair of said M binary bits in said kth orthogonal modulation code is equal to a Logic 00 value and is equal to Logic 0 otherwise; and

an input decision circuit capable of detecting a [+1,+1] signal output by said Logic 00 input detector after a comparison of a jth sequential pair of said M/2 sequential pairs of said M binary bits to a Logic 00 value and, in response to said detection, adding said [+1,+1] signal to a Kth one of said S accumulators in said summation circuit if a jth one of said M/2 Logic 00 code mask bits in said Kth Logic 00 code mask in said storage array is equal to Logic 1.

2. The demodulator as set forth in Claim 1 wherein said storage array is further capable of storing S Logic 01 code masks, each of said S Logic 01 code masks associated with one of said S possible orthogonal modulation codes, wherein a kth Logic 01 code mask comprises M/2 Logic 01 code mask bits, each of said M/2 Logic 01 code mask bits associated with a corresponding one of M/2 sequential pairs of M binary bits in a kth orthogonal modulation code, wherein said each M/2 Logic 01 code mask bit is a Logic 1 if said corresponding sequential pair of said M binary bits in said kth orthogonal modulation code is equal to a Logic 01 value and is equal to Logic 0 otherwise.

3. The demodulator as set forth in Claim 2 wherein said input decision circuit is further capable of detecting a [+1,+1] signal output by said Logic 01 input detector after a comparison of a jth sequential pair of said M/2 sequential pairs of said M binary bits to a Logic 01 value and, in response to said detection, adding said [+1,+1] signal to a Kth one of said S accumulators in said summation circuit if a jth one of said M/2 Logic 01 code mask bits in said Kth Logic 01 code mask in said storage array is equal to Logic 1.

4. The demodulator as set forth in Claim 3 wherein said storage array is further capable of storing S Logic 10 code masks, each of said S Logic 10 code masks associated with one of said S possible orthogonal modulation codes, wherein a kth Logic 10 code mask comprises M/2 Logic 10 code mask bits, each of said M/2 Logic 10 code mask bits associated with a corresponding one of M/2 sequential pairs of M binary bits in a kth orthogonal modulation code, wherein said each M/2 Logic 10 code mask bit is a Logic 1 if said corresponding sequential pair of said M binary bits in said kth orthogonal modulation code is equal to a Logic 10 value and is equal to Logic 0 otherwise.

5. The demodulator as set forth in Claim 4 wherein said input decision circuit is further capable of detecting a [+1,+1] signal output by said Logic 10 input detector after a comparison of a jth sequential pair of said M/2 sequential pairs of said M binary bits to a Logic 10 value and, in response to said detection, adding said [+1,+1] signal to a Kth one of said S accumulators in said summation circuit if a jth one of said M/2 Logic 10 code mask bits in said Kth Logic 10 code mask in said storage array is equal to Logic 1.

6. The demodulator as set forth in Claim 5 wherein said storage array is further capable of storing S Logic 11 code masks, each of said S Logic 11 code masks associated with one of said S possible orthogonal modulation codes, wherein a kth Logic 11 code mask comprises M/2 Logic 11 code mask bits, each of said M/2 Logic 11 code mask bits associated with a corresponding one of M/2 sequential pairs of M binary bits in a kth orthogonal modulation code, wherein said each M/2 Logic 11 code mask bit is a Logic 1 if said corresponding sequential pair of said M binary bits in said kth orthogonal modulation code is equal to a Logic 11 value and is equal to Logic 0 otherwise.

7. The demodulator as set forth in Claim 6 wherein said input decision circuit is further capable of detecting a [+1,+1] signal output by said Logic 11 input detector after a comparison of a jth sequential pair of said M/2 sequential pairs of said M binary bits to a Logic 11 value and, in response to said detection, adding said [+1,+1] signal to a Kth one of said S accumulators in said summation circuit if a jth one of said M/2 Logic 11 code mask bits in said Kth Logic 11 code mask in said storage array is equal to Logic 1.

8. The demodulator as set forth in Claim 7 further comprising a code selection circuit capable of reading a sum value from each said S accumulators and identifying an accumulator containing a maximum sum value.

9. The demodulator as set forth in Claim 8 wherein said code selection circuit outputs one of 2^M N-bit data symbols corresponding to said identified accumulator containing said maximum value.

10. The demodulator as set forth in Claim 9 wherein N = 6 and $M = 2^N = 64$.

11. The demodulator as set forth in Claim 10 wherein S = 64.

12. The demodulator as set forth in Claim 11 wherein said orthogonal modulation codes are Walsh codes.

13. A code division multiple access (CDMA) wireless network comprising a plurality of base transceiver stations capable of communicating with access terminals located in a coverage area of said wireless network, wherein a first one of said plurality of base transceiver stations comprises:

a demodulator for demodulating a set of S possible orthogonal modulation codes received serially as binary data, wherein each of said S possible orthogonal modulation codes comprises M binary bits representing an N-bit data symbol and wherein $M = 2^N$, said demodulator comprising:

a Logic 00 input detector, a Logic 01 input detector, a Logic 10 input detector and a Logic 11 input detector, wherein each of said Logic 00 input detector, said Logic 01 input detector, said Logic 10 input detector, and said Logic 11 input detector compares sequential pairs of said M binary bits of said serially received orthogonal modulation codes to a respective one of a Logic 00 value, a Logic 01 value, a Logic 10 value, and a Logic 11 value and outputs a [+1,+1] signal if a match occurs and outputs a [-1,-1] signal if a match does not occur;

a summation circuit comprising S accumulators;

a storage array capable of storing S Logic 00 code masks, each of said S Logic 00 code masks associated with one

of said S possible orthogonal modulation codes, wherein a kth Logic 00 code mask comprises M/2 Logic 00 code mask bits, each of said M/2 Logic 00 code mask bits associated with a corresponding one of M/2 sequential pairs of M binary bits in a kth orthogonal modulation code, wherein said each M/2 Logic 00 code mask bit is a Logic 1 if said corresponding sequential pair of said M binary bits in said kth orthogonal modulation code is equal to a Logic 00 value and is equal to Logic 0 otherwise; and

an input decision circuit capable of detecting a [+1,+1] signal output by said Logic 00 input detector after a comparison of a jth sequential pair of said M/2 sequential pairs of said M binary bits to a Logic 00 value and, in response to said detection, adding said [+1,+1] signal to a Kth one of said S accumulators in said summation circuit if a jth one of said M/2 Logic 00 code mask bits in said Kth Logic 00 code mask in said storage array is equal to Logic 1.

14. The CDMA wireless network as set forth in Claim 13 wherein said storage array is further capable of storing S Logic 01 code masks, each of said S Logic 01 code masks associated with one of said S possible orthogonal modulation codes, wherein a kth Logic 01 code mask comprises M/2 Logic 01 code mask bits, each of said M/2 Logic 01 code mask bits associated with a corresponding one of M/2 sequential pairs of M binary bits in a kth orthogonal modulation code, wherein said each M/2 Logic 01 code mask bit is a Logic 1 if said corresponding sequential pair of said M binary bits in said kth orthogonal modulation code is equal to a Logic 01 value and is equal to Logic 0 otherwise.

15. The CDMA wireless network as set forth in Claim 14 wherein said input decision circuit is further capable of detecting a [+1,+1] signal output by said Logic 01 input detector after a comparison of a jth sequential pair of said M/2 sequential pairs of said M binary bits to a Logic 01 value and, in response to said detection, adding said [+1,+1] signal to a Kth one of said S accumulators in said summation circuit if a jth one of said M/2 Logic 01 code mask bits in said Kth Logic 01 code mask in said storage array is equal to Logic 1.

16. The CDMA wireless network as set forth in Claim 15 wherein said storage array is further capable of storing S Logic 10 code masks, each of said S Logic 10 code masks associated with one of said S possible orthogonal modulation codes, wherein a kth Logic 10 code mask comprises M/2 Logic 10 code mask bits, each of said M/2 Logic 10 code mask bits associated with a corresponding one of M/2 sequential pairs of M binary bits in a kth orthogonal modulation code, wherein said each M/2 Logic 10 code mask bit is a Logic 1 if said corresponding sequential pair of said M binary bits in said kth orthogonal modulation code is equal to a Logic 10 value and is equal to Logic 0 otherwise.

17. The CDMA wireless network as set forth in Claim 16 wherein said input decision circuit is further capable of detecting a [+1,+1] signal output by said Logic 10 input detector after a comparison of a jth sequential pair of said M/2 sequential pairs of said M binary bits to a Logic 10 value and, in response to said detection, adding said [+1,+1] signal to a Kth one of said S accumulators in said summation circuit if a jth one of said M/2 Logic 10 code mask bits in said Kth Logic 10 code mask in said storage array is equal to Logic 1.

18. The CDMA wireless network as set forth in Claim 17 wherein said storage array is further capable of storing S Logic 11 code masks, each of said S Logic 11 code masks associated with one of said S possible orthogonal modulation codes, wherein a kth Logic 11 code mask comprises M/2 Logic 11 code mask bits, each of said M/2 Logic 11 code mask bits associated with a corresponding one of M/2 sequential pairs of M binary bits in a kth orthogonal modulation code, wherein said each M/2 Logic 11 code mask bit is a Logic 1 if said corresponding sequential pair of said M binary bits in said kth orthogonal modulation code is equal to a Logic 11 value and is equal to Logic 0 otherwise.

19. The CDMA wireless network as set forth in Claim 18 wherein said input decision circuit is further capable of detecting a [+1,+1] signal output by said Logic 11 input detector after a comparison of a jth sequential pair of said M/2 sequential pairs of said M binary bits to a Logic 11 value and, in response to said detection, adding said [+1,+1] signal to a Kth one of said S accumulators in said summation circuit if a jth one of said M/2 Logic 11 code mask bits in said Kth Logic 11 code mask in said storage array is equal to Logic 1.

20. The CDMA wireless network as set forth in Claim 19 further comprising a code selection circuit capable of reading a sum value from each said S accumulators and identifying an accumulator containing a maximum sum value.

21. The CDMA wireless network as set forth in Claim 20 wherein said code selection circuit outputs one of 2^M N-bit data symbols corresponding to said identified accumulator containing said maximum value.

22. The CDMA wireless network as set forth in Claim 21 wherein $N = 6$ and $M = 2^N = 64$.

23. The CDMA wireless network as set forth in Claim 22 wherein $S = 64$.

24. The CDMA wireless network as set forth in Claim 23 wherein said orthogonal modulation codes are Walsh codes.